QuantaGrid D51B-1U

Revision 1.0

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Revision History:

Revision	Date	Description
1.0	2015-11-04	Release for Open Compute Project

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1 INTRODUCTION

The S2B will be IA-64 based dual-socket servers that support the Grantley –EP processors in combination with the Wellsburg PCH (PCH) to provide a balanced feature set between technology leadership and cost. Quanta Grantley will be 24 DIMM and three x16 risers,

The intended audiences for this document are the Grantley platform technical leads, software team, validation team, and board design engineers that need to utilize a comprehensive package. This document will provide the S2B Design Teams the product specific features that are required to be implemented on the boards. Product feature requirements and block diagrams will be provided.

Links to reference documents that dive into the implementation for the software stack, common-core solution, server management architecture, fan-speed control architecture, chassis, power budget, and thermal requirements are provided.

2 PRODUCT ARCHITECTURE OVERVIEW

The S2B 24 DIMMs Server board will be Quanta Grantley server product. The silicon ingredients and features are as follows list:

Table 2-1. Grantley Enterprise Server S2B Feature List

Board Name	**Grantley Server Baseboard**
Form Factor	2U Rack (X2M chassis)/ 720mm x 430mm x 87.5mm/ 28.34" x 16.92" x 3.4" 1U Rack (X1S chassis) / 720mm x 430mm x 43.5mm/ 28.34" x 16.92" x 1.7"
Baseboard size	16.7” x 16”, 8 layer, 2.4mm, 24 DIMMs
CPU	Intel Haswell E5-2600V3, -R3 Socket
Max Processor Wattage	145W, Optimized power delivery for 95W, VRD 12.5
QPI Speed	9.6 GT/s, 8.0GT/s, 6.4GT/s
Chipset	Intel (R) C610 series chipset (Wellsburg)
Memory	ECC RDIMM/ LRDIMM slots Up to 768GB (32Gx24) of memory for LRDIMM Up to 768GB (32Gx24) of memory for RDIMM
PCIe Expansion Slot	**1U Chassis** (1) PCIe x16 G3 riser slot for low-profile card (By Riser1) (1) PCIe x16 G3 riser slot for full height card (By Riser2) (1) PCIe x8 G3 OCP mezzanine card slot **2U Chassis** (2) PCIe x8 G3 riser slot for low-profile card + (1) PCIe x8 G3 Linking slot for low-profile card (By Riser1, Default) (1) PCIe x16 G3 riser slot for low-profile card + (1) PCIe x8 G3 riser slot for low-profile card (By Riser1, Option) (1) PCIe x16 G3 riser slot for full height card + (1) PCIe x8 G3 riser slot for Full height card (By Riser2) (1) PCIe x8 G3 OCP mezzanine card slot
Rear IO	(2) USB 3.0 ports (1) VGA port (BMC AST2400 SKU only) (1) RS232 serial port (2) GbE or 10G BASE-T RJ45 ports (1) GbE RJ45 management port (1) ID LED (1) Port80 Debug Port (option)

Front IO	Power/ID/Reset Buttons, LEDs (2) USB 2.0 ports
Network	Powerville Dual GbE: (2 MACs and 2 PHYs Integrated) Twinville Dule 10GbE (Option) PHY RTL8211 to BMC for delicate management NIC port.
Storage	(24) 2.5" or (12) 3.5" SATA/SAS hot-plug drives (2U Chassis) (10) 2.5" or (4) 3.5" SATA/SAS hot-plug drives (1U Chassis) (2) SATADOM (optional) (2) 2.5" hot-plug SAS or PCIe SSDs (optional)
USB	Two USB3.0 ports on Rear Two USB2.0 ports on Front panel (Option)
Video	ASPEED AST2400 8MB DDR3 video memory
Series Port	One external serial port on Rear One internal serial port (Option)
FAN	1U 6 dual-rotor FAN connectors from HDD backplane. 2U 4 dual-rotor FAN connectors on motherboard
ACPI	ACPI compliance, S0, S5 support. (* No S1 and S3 support.)
TPM	Yes (Option)
Power-Supply	(2) 1100W high efficiency redundant PSU, 100-240VAC 50/60Hz (2U Chassis) Or (2) 750W high efficiency redundant PSU, 100-240VAC 50/60Hz (1U Chassis)
Chassis	1U system / 2U system

2.1 PRODUCT ARCHITECTURE BLOCK DIAGRAM

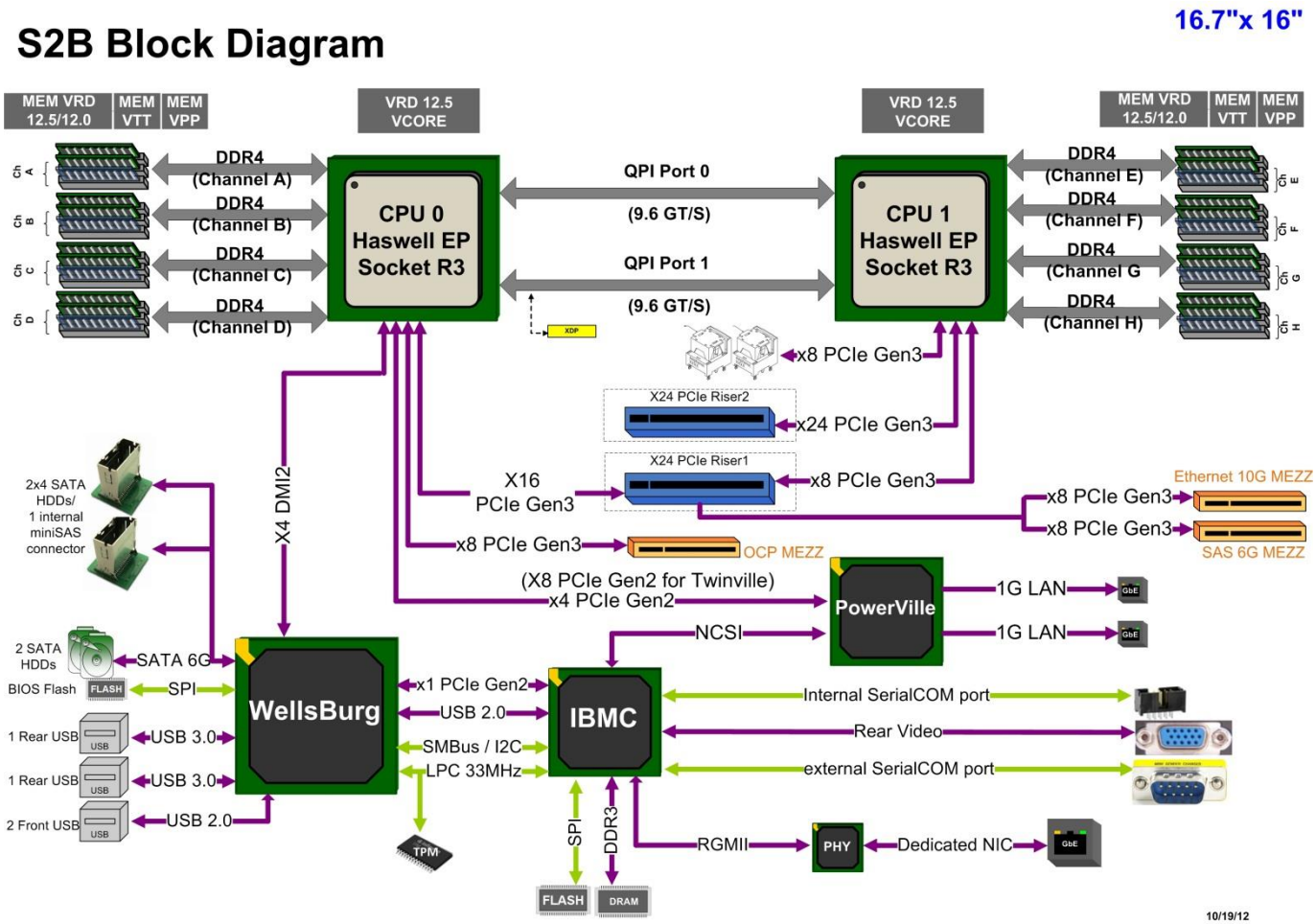

Figure 2-1 Grantley Enterprise Rack S2B Configuration

2.2 BASEBOARD PLACEMENT

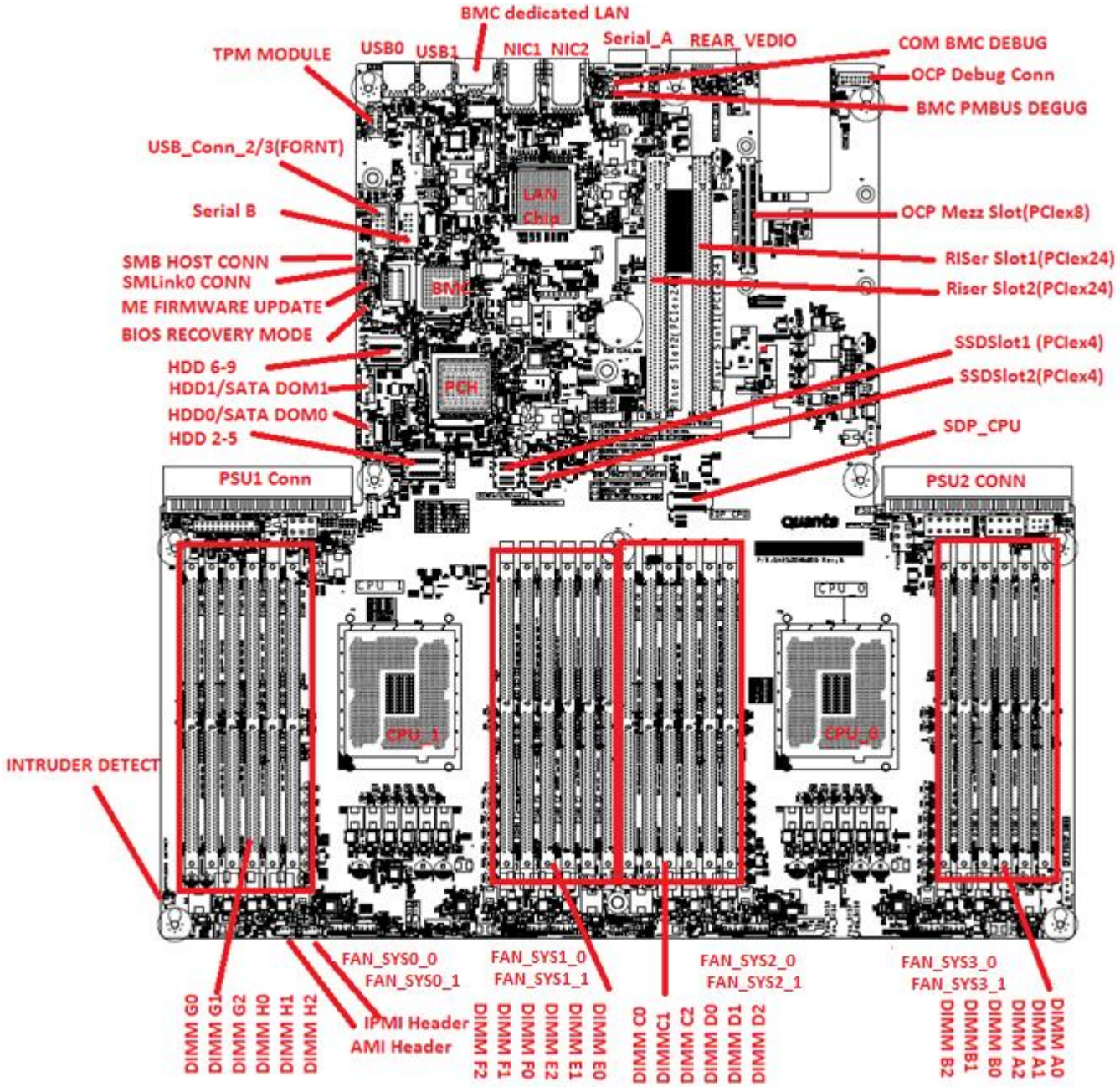

Figure 2-2: Quanta Grantley 2S 24-DIMM S2B Baseboard Placement

2.3 BASEBOARD Diemesion

W 425mm (16.7 “) x L 406mm (16”)

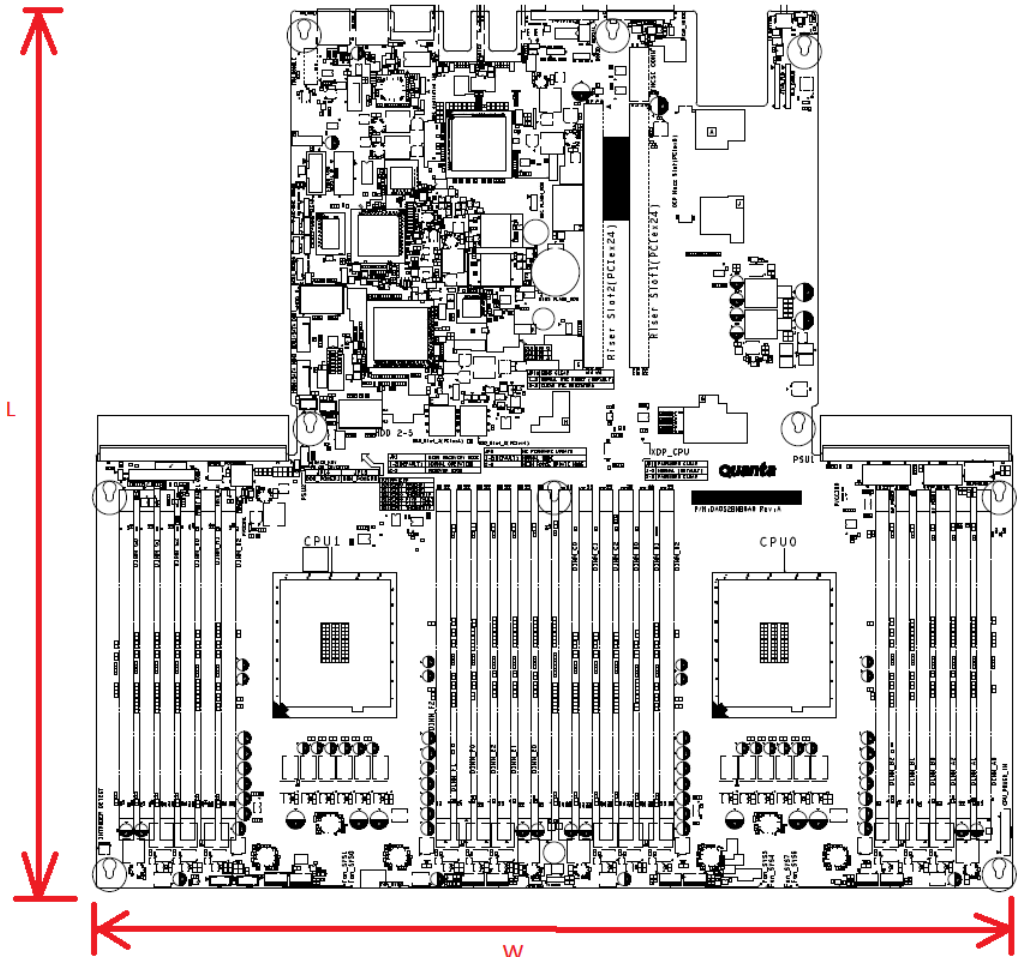

Figure 2-3: Quanta Grantley 2S 24-DIMM S2B BaseBoard Dimension

3 PRODUCT FEATURES

3.1 PROCESSOR

The Processor's core name of Grantley platform is named "Haswell EP Processor- E5-2600V3". It is 22nm process Processor with new Microarchitecture and New Instructions (including AVX 2.0). And the processor supports 4 DDR4 Memory channels. The QPI bus speed has improved up to 9.6GT/s. In this generation, the processor has internal voltage regulator (IVR), IVR integrates legacy power delivery onto processor package/die. So IVR enables power management benefits and simplified platform power design.

3.2 MEMORY

Quanta Grantley Server board S2B support total 24 DDR4 DIMMs.

3.2.1 DIMM NOMENCLATURE

DIMMs are organized into physical slots on DDR4 memory channels that belong to processor sockets. The memory channels from Socket 0 (CPU-0) are identified as Channel A, B, C, D. The memory channels from Socket 1 (CPU-1) are identified as Channel E, F, G and H.

The DIMM identifiers on the silkscreen on the board provide information about the channel, and therefore the processor, to which they belong. For example, DIMM_A0 is the first slot on Channel A of processor 0; DIMM_E0 is the first DIMM socket on Channel A of processor 1.

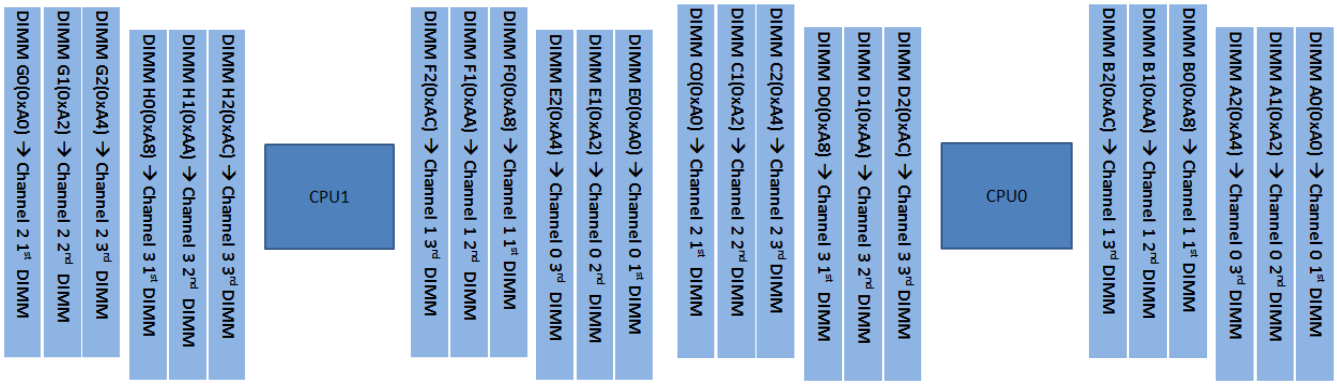

Figure 3-1 processor SKU list

3.3 PCH

The PCH's core name of Grantley platform is named "Wellsburg".

Wellsburg Key Features:

- Optimized and Validated to work with Haswell Server CPUs
- Integrated system clocks w/ support for ext. clock buffers
- Reduced TDP / Average Power/ Package (vs. Patsburg)
- Intel® SVT / Dengate* support capable
- USB3 XHCI Debug Device required for Windows8
- Flexible Management Infrastructure focused on Run Time
- Support for MCTP Protocol and End Points
- Support for Management traffic over DMI
- Embedded Platform SW Services capability
- 6x SMBus; 1@ 1MHz bus support for LAN or BMC
- SPI Enhancements (large enough address space for 2 BIOS)
- Continued support for GSX (GPIO Expansion slots)
- 10 SATA ports capable of 6Gb/s
- Up to 6 ports of USB3; 8 ports of USB2
- Up to 8 x1 PCIe G2
- Intel ® Node Manager 3.0 (with BE, EE options)
- vPro/AMT
- RSTe SW RAID (optional DSS SSD caching capability)

3.3.1 PCH GPIOs

Table 3-3. PCH GPIOs List

Item	Pin Name	Signal Name	Usage	Strapping	In/Out
GPIO0	BMBUSY_N_GPIO0	PU_PCH_GPIO0	No used and PU to P3V3		In
GPIO1	TACH1_GPIO1	REVISION_ID1	REVISION_ID1		In
GPIO2	PIRQE_N_GPIO2	FM_CPU_ERR0_CO_N	Error seen signaling from CPU		In
GPIO3	PIRQF_N_GPIO3	FM_ERR1_DLY_N	Error seen signaling from CPLD (Delay)		In
GPIO4	PIRQG_N_GPIO4	PU_PIRQG_N	No used and PU to P3V3		In
GPIO5	PIRQH_N_GPIO5	IRQ_CPU_CATERR_DLY	CATERR_N RC delay		In
GPIO6	TACH2_GPIO6	TP_BOARD_ID0	NA		In
GPIO7	TACH3_GPIO7	TP_BOARD_ID1	NA		In
GPIO8	GPIO8	IRQ_BMC_PCH_NMI_N_MUX	NMI form BMC	**Integrated Clock Chip Enable / Disable** 0 = Enable Integrated Clock Chip mode. 1 = Disable Integrated Clock Chip mode.[Default]	In
GPIO9	OC5_N_GPIO9	FP_PWR_LED_N	Turn on PWR LED on FP		Out
GPIO10	OC6_N_GPIO10	FM_TPM_PRSNT_N	Detect TPM		In
GPIO11	SMBALERT_N_GPIO11	RST_PCIE_CPU_N			Out
GPIO12	LAN_PHY_PWR_CTRL_GPIO12	IRQ_IBMC_PCH_SMI_LPC_N	SMI from BMC		In
GPIO13	GPIO13	FM_IBMC_PCH_SCI_LPC_N	SCI from BMC		In
GPIO14	OC7_N_GPIO14	PU_USB_OC7_R_N	No used and PU to P3V3_AUX		In
GPIO15	GPIO15	FM_PCH_SATA_RAID_KEY	SATA RAID KEY		In
GPIO16	SATA4GP_GPIO16_MGPIO9	FM_THROTTLE_N	THROTTLE		Out
GPIO17	TACH0_GPIO17	REVISION_ID0	REVISION_ID0		In
GPIO18	GPIO18	PU_PCH_GPIO18	No used and PU to P3V3		In

GPIO19	SATA1GP_GPIO19	RST_PCIE_PCH_N	Reset PCIE	**Boot BIOS Strap bit 0** Bit1 Bit0 Boot BIOS Destination 0 1 Reserved 1 0 RSVD 1 1 SPI [Default] 0 0 LPC	In
GPIO20	GPIO20_SMI_N	PU_PCH_GPIO20	No used and PU to P3V3		Out
GPIO21	SATA0GP_GPIO21	PD_SATA0GP_GPIO21	No used and PD to GND		In
GPIO22	SCLOCK_GPIO22	SGPIO_SATA_CLOCK_R	SGPIO SATA CLOCK		Out
GPIO23	LDRQ1_N_GPIO23	TP_PCH_LDRQ1_N	No used and TP		In
GPIO24	GPIO24_MGPIO0	PU_PCH_GPIO24	No used and PU to P3V3_AUX		In
GPIO25	GPIO25	FM_PCH_LAN0_DISABLE_N	DISABLE LAN		Out
GPIO26	GPIO26	PU_PCH_GPIO26	No used and PU to P3V3_AUX		In
GPIO27	GPIO27_MGPIO6	FM_VIDEO_DISABLE_N	Video output enable/disable indicate from PCH		Out
GPIO28	GPIO28_MGPIO7	FM_USB_EN_N	Enable USB PWR		Out
GPIO29	SLP_WLAN_N_GPIO29_MGPIO3	PU_PCH_GPIO29	No used and PU to P3V3_AUX		In
GPIO30	SUSWARN_N_GPIO30_MGPIO1	PU_PCH_GPIO30	No used and PU to P3V3_AUX		In
GPIO31	GPIO31_MGPIO2	IRQ_SML1_PMBUS_ALERT_N	PMBus Alert from PSU1 and PSU2		In
GPIO32	GPIO32	PU_PCH_GPIO32	No used and PU to P3V3		In
GPIO33	GPIO33	FM_QPI_SLOW_MODE_N	QPI SLOW MODE SELECT	**DMI TX Termination** 0 = DMI TX is terminated to VSS. 1 = DMI TX is terminated to VCC. [Default]	In
GPIO34	GPIO34	OCP_MEZZA_PRSNT_N	Detect OCP MEZZA		In
GPIO35	GPIO35_NMI_N	FM_NMI_EVENT_2_N	Inform BMC NMI EVENT		In
GPIO36	SATA2GP_GPIO36	FM_BIOS_ADV_FUNCTIONS	BIOS ADVANCED FUNCTIONS	**DMI RX Termination** 0 = DMI RX is terminated to	In

				VSS. 1 = DMI RX is terminated to common mode. [Default]	
GPIO37	SATA3GP_GPIO37	PU_ADR_TRIGGER_N	TLS CONFIDENTIALITY ENABLE	**TLS Confidentiality** 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality) 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality) [Default]	In
GPIO38	SLOAD_GPIO38	SGPIO_SATA_LOAD_R	SGPIO SATA LOAD		Out
GPIO39	SDATAOUT0_GPIO39	SGPIO_SATA_DATAOUT0_R	SGPIO SATA DATAOUT0		Out
GPIO40	OC1_N_GPIO40	FM_USB_OC1_BP_R_N	USB OVER CURRENT		In
GPIO41	OC2_N_GPIO41	PU_USB_OC2_R_N	No used and PU to P3V3_AUX		In
GPIO42	OC4_N_GPIO42	ROMA<0>	Disable BMC		Out
GPIO43	OC4_N_GPIO43	FM_USB_OC4_FP_R_N	USB OVER CURRENT		In
GPIO44	GPIO44	FM_PCH_LAN1_DISABLE_N	DISABLE LAN		Out
GPIO45	GPIO45	RST_PCH_IBMC_N	RST BMC		Out
GPIO46	GPIO46	FM_BIOS_POST_CMPLT_N	For BIOS to indicate POST status to BMC		In
GPIO47	GPIO47	FM_BMC_READY_N	BMC ready indicate to PCH		In
GPIO48	SDATAOUT1_GPIO48	SGPIO_SATA_DATAOUT1_R	SGPIO SATA DATAOUT1		Out
GPIO49	SATA5GP_GPIO49_MGPIO10	FM_CPU_PROCHOT_N	Detect CPU PROCHOT		In
GPIO50	GPIO50_GSXCLK	FM_RISER2_CFG1	Riser2 PCIE configuration		In
GPIO51	GPIO51_GSXDOUT	PD_SGPIO_GSX_DOUT	No used and PD to GND	**Boot BIOS Strap bit 1** Bit1 Bit0 Boot BIOS Destination 0 1 Reserved 1 0 RSVD	In

				1 1 SPI [Default] 0 0 LPC	
GPIO52	GPIO52_GSXSLOAD	FM_RISER2_CFG0	Riser2 PCIE configuration		In
GPIO53	GPIO53_GSXDIN	PD_SGPIO_GSX_MUX_DIN	No used and PD to GND	**DMI AC Coupling** 0= Configures DMI for AC coupling mode. 1 = Configures DMI for DC coupling mode. [Default]	In
GPIO54	GPIO54_GSXSRESET_N	FM_RISER1_CFG0	Riser1 PCIE configuration		In
GPIO55	GPIO55	PU_PCH_GPIO55	No used and PU to P3V3	**Top-Block Swap Override** 0 = Enable “Top-Block Swap” mode - PCH will invert A16 for cycles going to the upper two 64 KB blocks in the FWH or appropriate address lines (A16, A17, A18, A19 or A20) as selected in BIOS Boot-Block size soft strap for SPI. 1 = Disable “Top-Block Swap” mode.. [Default]	In
GPIO56	GPIO56	FM_BIOS_RCVR_BOOT_N	BIOS RECOVERY MODE		In
GPIO57	GPIO57_MGPIO5	FM_ME_RCVR_N	ME FIRMWARE UPDATE		in
GPIO58	SML1CLK_GPIO58_MGPIO11	SMB_3V3SB_PMBUS_CLK_R	SM bus CLK		Out
GPIO59	OC0_N_GPIO59	PU_USB_OC0_R_N	No used and PU to P3V3		In
GPIO60	SML0ALERT_N_GPIO60_MGPIO4	IRQ_SML0ALERT_N	SM bus Alert to BMC		Out
GPIO61	SUS_STAT_N_GPIO61	PU_PCH_GPIO61	CPLD JTAG TDI		Out
GPIO62	SUSCLK_GPIO62	CLK_33K_SUSCLK	CLK 33MHZ	**PLL On-Die Voltage Regulator Enable** 0 = Disable PLL On-Die voltage regulator. 1 = Enable PLL On-Die voltage regulator.[Default]	Out

GPIO63	SLP_S5_N_GPIO63	PU_SLP_S5_N	No used and reserve a PU to P3V3_AUX		Float
GPIO64	CLKOUTFLEX0_GPIO64	FM_RISER1_CFG1	Riser1 PCIE configuration		In
GPIO65	CLKOUTFLEX1_GPIO65	SLOT3_PRESENT_N	Detect SLOT3		In
GPIO66	CLKOUTFLEX2_GPIO66	SLOT2_PRESENT_N	Detect SLOT2		In
GPIO67	CLKOUTFLEX3_GPIO67	SLOT1_PRESENT_N	Detect SLOT1		In
GPIO68	TACH4_GPIO68	TP_BOARD_ID2	NA		In
GPIO69	TACH5_GPIO69	TP_BOARD_ID3	NA		In
GPIO70	TACH6_GPIO70	TP_BOARD_ID4	NA		In
GPIO71	TACH7_GPIO71	TP_BOARD_ID5	NA		In
GPIO72	GPIO72	PU_PCH_GPIO72	No used and PU to P3V3_AUX		In
GPIO73	GPIO73	PU_PCH_GPIO73	No used and PU to P3V3_AUX		In
GPIO74	SML1ALERT_N_PCHHOT_N_GPIO74_MGPIO8	FM_PCH_BMC_THERMTRIP_N	PCH HOT indicate		Out
GPIO75	SML1DATA_GPIO75_MGPIO12	SMB_3V3SB_PMBUS_DAT_R	SM bus DATA		Bi
HDA_SDO	HDA_SDO	AUD_AZA_SDO	Reserve PU to P3V3_AUX	**Flash Descriptor Security Override** 0 = Enable security measures defined in the Flash Descriptor. [default] 1 = Disable Flash Descriptor Security (override).	Out
INTVRMEN	INTVRMEN	PU_PCH_INTVRMEN	Enable internal VRM	Integrated VRM Enable 0 = Disable 1 = Enable [Default]	In
DSWVRMEN	DSWVRMEN	PU_PCH_DSWODVREN	Deep Sx Well On-Die Voltage Regulator Enable	**Deep Sx Well On-Die Voltage Regulator Enable** 0 = Disable Integrated DeepSx Well (DSW) On-Die Voltage Regulator. 1 = Enable DSW 3.3V-to-1.05V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. [Default]	In

SPKR	SPKR	SPEAKER_PCH	Control speaker	**No Reboot** 0 = Disable “No Reboot” mode. 1 = Enable “No Reboot” mode. [Default]	Out
MEXP_SMBDATA0	MEXP_SMBDATA_0	SMB_MEXP_SMBDATA_0	SMB SDA	**ADR Timer Hold off** 0 = Enable 1 = Disable [Default]	I/OD
MEXP_SMBDATA1	MEXP_SMBDATA_1	PU_MEXP_SMBDATA_1	SMB SDA	**LT Key Downgrade** 0 = Enable 1 = Disable [Default]	I/OD

3.4 BMC

There are 2 BMC options on the S2B Mainboard – AST2400 which include VGA interface.

3.4.1 AST2400 (Default)

The Server's Board Management Controller (**AST2400**) is a highly integrated single-chip solution, integrating several devices typically found on servers.

3.5 CLOCKS

The Grantley platform has two different clock architectures, external clock architecture (exCLK) and integrated system clock (isCLK) architecture. The Wellsburg PCH is capable of providing both exCLK and isCLK. S2B will use Hybrid clock mode. The external clock generator is not needed. There is a clock generator is from PCH internal and an external clock buffer.

S2B Clock Diagram

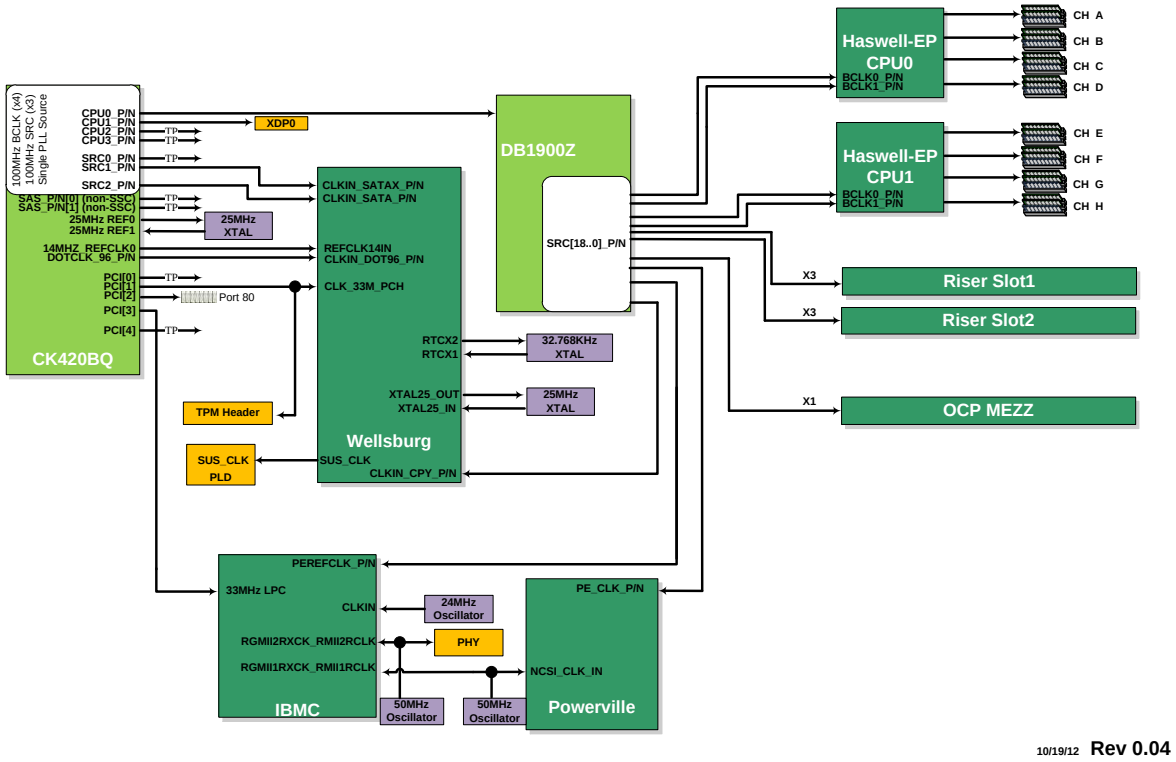

Figure 3-4: Grantley Product System Clock Diagram

3.6 SATA

The Wellsburg PCH supports total 10 SATA-III 6Gbs ports. The PCH contains three SATA controller modes, while IDE, ACHI and Raid mode.

The project supports 6 SATAIII ports, while two 7 pins SATA ports on baseboard, 4 SATA ports connect to internal miniSAS Connector for system HDD backplane connection.

3.6.1 SATA PORT CONNECTIVITY

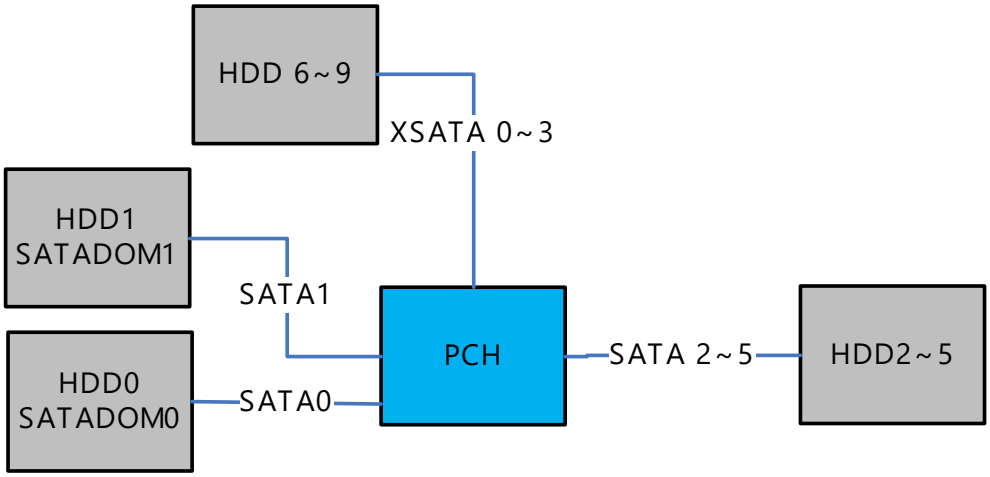

Figure 3-6: S2B SATA Diagram

3.7 USB

The Wellsburg PCH supports total 14 USB ports, 6 USB 2.0 ports and 8 USB 3.0 ports. The USB port distribution of Quanta Grantley product is as follows:

- ASPEED BMC AST2400 consumes 2 USB 2.0 ports (one 1.1 and one 2.0)
- 2 Rear USB3.0 ports are needed for this project
- 2 Front-panel USB2.0 ports are needed for 1U 3.5” SKU and 2U chassis

The USB ports on the products are not required to be powered from STBY.

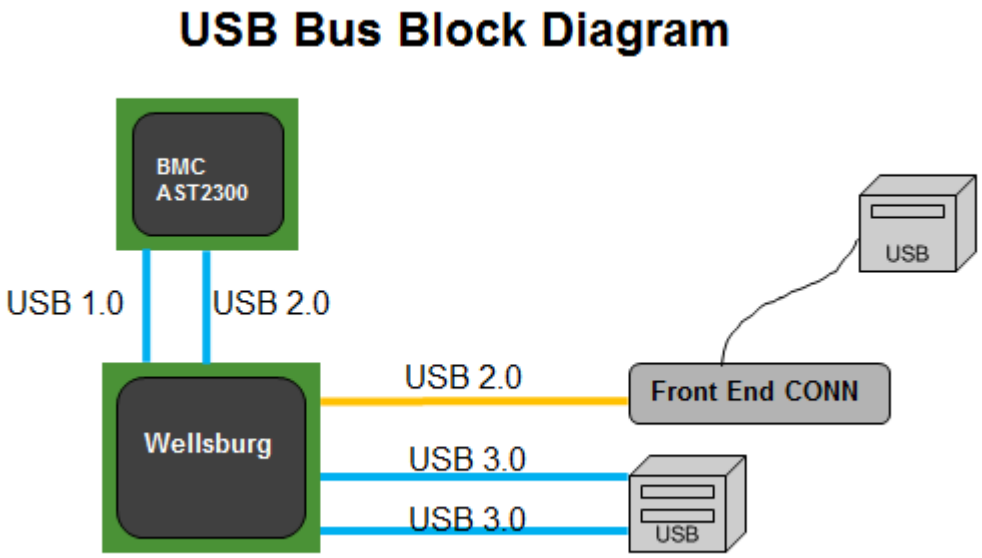

Figure 3-7: Grantley USB Ports

3.8 PCIe BUS

PCI Express* Gen1, Gen2 and Gen 3 are dual-simplex point-to point serial differential low-voltage interconnects. The signaling bit rate is 2.5 Gb/s one direction per lane for Gen1 (8b/10b encoding), 5.0 Gbit/s one direction per lane for Gen2 (8b/10b encoding) and 8.0 Gb/s one direction per lane for Gen3 (128b/130b encoding). Each port consists of a transmitter and receiver pair. A link between the ports of two devices is a collection of lanes (x1, x2, x4, x8, x16, etc.).

3.8.1 PCIe PORT CONNECTIVITY

The following diagram lists the usage of the Grantley-EP and Wellsburg PCIe bus segments in S2B project.

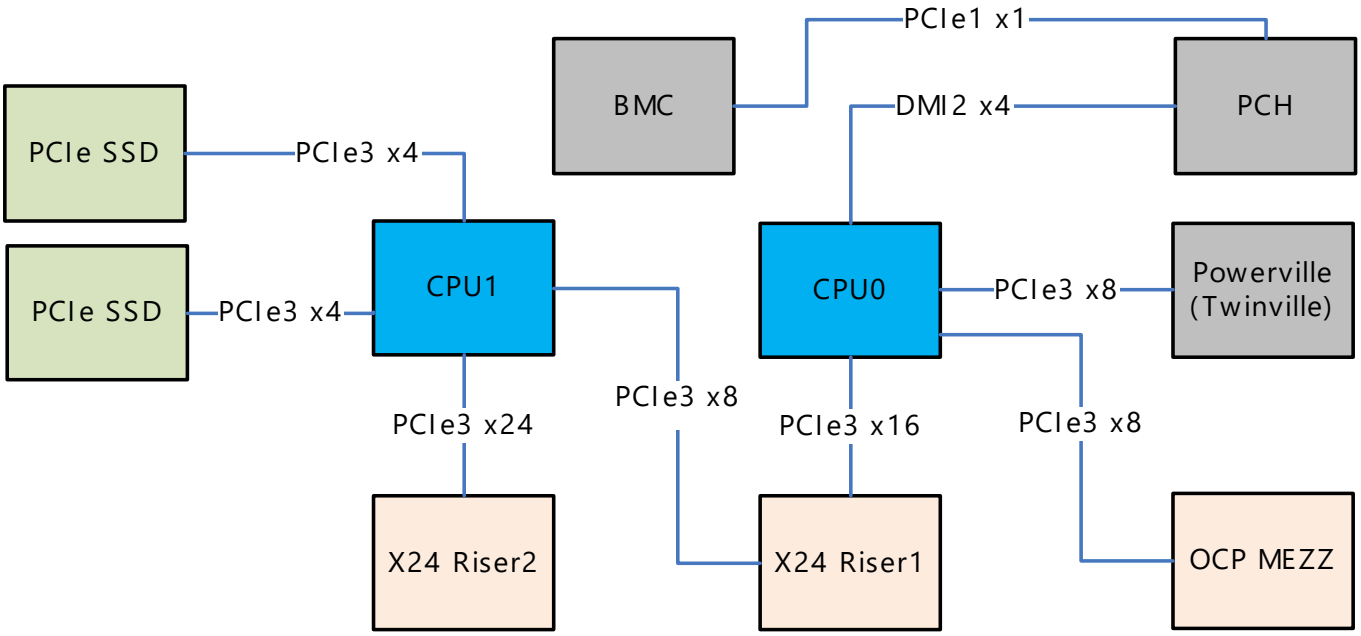

Figure 3-8 Quanta Grantley S2B PCIe block diagram

3.9 PCIe Interface

There are multi types of Riser boards and Mezzanine boards for this project. Also we will have PCIe SSD Backplane connected to motherboard via Cable. The follow table lists the detail request of this project.

Table 3-8. Riser and Mezzanine list

Description		
1U	1 Slot Riser1	Support (1) PCIe Gen3 x8 Add-on Card
	1 Slot Riser2	Support (1) PCIe GEN3 x16 Add-on Card
	Linking Riser1	Support (1) PCIe Gen3 x8 Link to Quanta LAN MEZZ Card (NCSI interface support)
2U	Riser1 – (2) Slot	Support (1) PCIe Gen3 x16 Add-on Card (1) PCIe Gen3 x8 Add-on Card
	Riser1 - (2) Slot +(1) linking	Support (1) PCIe Gen3 x8 linking slot (NCSI interface support) (2) PCIe Gen3 x8 Add-on Card
	Riser2 - (2) Slot	Support (1) PCIe Gen3 x16 slot (1) PCIe Gen3 x8 Add-on Card
OCP Mezz		PCIe x8 Connector NCSI interface support
PCIe SSD		Support (2) PCIe Gen3 x4 port for PCIe SSD Drive

3.9.1 Riser Slot PINOUT

3.9.1.1 Riser 1 PINOUT Definition

Table 3-9. PIN definition of PCIe Riser 1

Riser 1			
Name	PIN		Name
P12V	B1	A1	GND
P12V	B2	A2	P12V
P12V	B3	A3	P12V
GND	B4	A4	P12V
P3V3	B5	A5	GND
P3V3	B6	A6	P3V3
P3V3	B7	A7	P3V3
P3V3	B8	A8	P3V3
GND	B9	A9	P3V3
P3V3_AUX	B10	A10	P3V3
IRQ_LVC3_WAKE_N	B11	A11	GND
P12V_STBY	B12	A12	RST_PERST0_N
SMB_PCI_3V3SB_CLK	B13	A13	SLOT1_PRESENT_N
SM B_PCI_3V3SB_DAT_SLOT1	B14	A14	FM_RISER1_CFG0
GND	B15	A15	FM_RISER1_CFG1
CLK_100M_PE1_DP	B16	A16	GND
CLK_100M_PE1_DN	B17	A17	CLK_100M_PE2_DP
GND	B18	A18	CLK_100M_PE2_DN
CLK_100M_PE3_DP	B19	A19	GND
CLK_100M_PE3_DN	B20	A20	P3E_CPU1_PCIE3_RX_DP7
GND	B21	A21	P3E_CPU1_PCIE3_RX_DN7
P3E_CPU1_PCIE3_TX_C_DP7	B22	A22	GND
P3E_CPU1_PCIE3_TX_C_DN7	B23	A23	GND
GND	B24	A24	P3E_CPU1_PCIE3_RX_DP6
GND	B25	A25	P3E_CPU1_PCIE3_RX_DN6
P3E_CPU1_PCIE3_TX_C_DP6	B26	A26	GND
P3E_CPU1_PCIE3_TX_C_DN6	B27	A27	GND
GND	B28	A28	P3E_CPU1_PCIE3_RX_DP5
GND	B29	A29	P3E_CPU1_PCIE3_RX_DN5
P3E_CPU1_PCIE3_TX_C_DP5	B30	A30	GND

P3E_CPU1_PCIE3_TX_C_DN5	B31	A31	GND
GND	B32	A32	P3E_CPU1_PCIE3_RX_DP4
GND	B33	A33	P3E_CPU1_PCIE3_RX_DN4
P3E_CPU1_PCIE3_TX_C_DP4	B34	A34	GND
P3E_CPU1_PCIE3_TX_C_DN4	B35	A35	GND
GND	B36	A36	P3E_CPU1_PCIE3_RX_DP3
GND	B37	A37	P3E_CPU1_PCIE3_RX_DN3
P3E_CPU1_PCIE3_TX_C_DP3	B38	A38	GND
P3E_CPU1_PCIE3_TX_C_DN6	B39	A39	GND
GND	B40	A40	P3E_CPU1_PCIE3_RX_DP2
GND	B41	A41	P3E_CPU1_PCIE3_RX_DN2
P3E_CPU1_PCIE3_TX_C_DP2	B42	A42	GND
P3E_CPU1_PCIE3_TX_C_DN2	B43	A43	GND
GND	B44	A44	P3E_CPU1_PCIE3_RX_DP1
GND	B45	A45	P3E_CPU1_PCIE3_RX_DN1
P3E_CPU1_PCIE3_TX_C_DP1	B46	A46	GND
P3E_CPU1_PCIE3_TX_C_DN1	B47	A47	GND
GND	B48	A48	P3E_CPU1_PCIE3_RX_DP0
GND	B49	A49	P3E_CPU1_PCIE3_RX_DN0
P3E_CPU1_PCIE3_TX_C_DP0	B50	A50	GND
P3E_CPU1_PCIE3_TX_C_DN0	B51	A51	GND
GND	B52	A52	P3E_CPU0_PCIE2_RX_DP15
GND	B53	A53	P3E_CPU0_PCIE2_RX_DN15
P3E_CPU0_PCIE2_TX_C_DP15	B54	A54	GND
P3E_CPU0_PCIE2_TX_C_DN15	B55	A55	GND
GND	B56	A56	P3E_CPU0_PCIE2_RX_DP14
GND	B57	A57	P3E_CPU0_PCIE2_RX_DN14
P3E_CPU0_PCIE2_TX_C_DP14	B58	A58	GND
P3E_CPU0_PCIE2_TX_C_DN14	B59	A59	GND
GND	B60	A60	P3E_CPU0_PCIE2_RX_DP13
GND	B61	A61	P3E_CPU0_PCIE2_RX_DN13
P3E_CPU0_PCIE2_TX_C_DP13	B62	A62	GND
P3E_CPU0_PCIE2_TX_C_DN13	B63	A63	GND
GND	B64	A64	P3E_CPU0_PCIE2_RX_DP12
GND	B65	A65	P3E_CPU0_PCIE2_RX_DN12
P3E_CPU0_PCIE2_TX_C_DP12	B66	A66	GND

P3E_CPU0_PCIE2_TX_C_DN12	B67	A67	GND
GND	B68	A68	P3E_CPU0_PCIE2_RX_DP11
GND	B69	A69	P3E_CPU0_PCIE2_RX_DN11
P3E_CPU0_PCIE2_TX_C_DP11	B70	A70	GND
P3E_CPU0_PCIE2_TX_C_DN11	B71	A71	GND
GND	B72	A72	P3E_CPU0_PCIE2_RX_DP10
GND	B73	A73	P3E_CPU0_PCIE2_RX_DN10
P3E_CPU0_PCIE2_TX_C_DP10	B74	A74	GND
P3E_CPU0_PCIE2_TX_C_DN10	B75	A75	GND
GND	B76	A76	P3E_CPU0_PCIE2_RX_DP9
GND	B77	A77	P3E_CPU0_PCIE2_RX_DN9
P3E_CPU0_PCIE2_TX_C_DP9	B78	A78	GND
P3E_CPU0_PCIE2_TX_C_DN9	B79	A79	GND
GND	B80	A80	P3E_CPU0_PCIE2_RX_DP8
GND	B81	A81	P3E_CPU0_PCIE2_RX_DN8
P3E_CPU0_PCIE2_TX_C_DP8	B82	A82	GND
P3E_CPU0_PCIE2_TX_C_DN8	B83	A83	GND
GND	B84	A84	P3E_CPU0_PCIE2_RX_DP7
GND	B85	A85	P3E_CPU0_PCIE2_RX_DN7
P3E_CPU0_PCIE2_TX_C_DP7	B86	A86	GND
P3E_CPU0_PCIE2_TX_C_DN7	B87	A87	GND
GND	B88	A88	P3E_CPU0_PCIE2_RX_DP6
GND	B89	A89	P3E_CPU0_PCIE2_RX_DN6
P3E_CPU0_PCIE2_TX_C_DP6	B90	A90	GND
P3E_CPU0_PCIE2_TX_C_DN6	B91	A91	GND
GND	B92	A92	P3E_CPU0_PCIE2_RX_DP5
GND	B93	A93	P3E_CPU0_PCIE2_RX_DN5
P3E_CPU0_PCIE2_TX_C_DP5	B94	A94	GND
P3E_CPU0_PCIE2_TX_C_DN5	B95	A95	GND
GND	B96	A96	P3E_CPU0_PCIE2_RX_DP4
GND	B97	A97	P3E_CPU0_PCIE2_RX_DN4
P3E_CPU0_PCIE2_TX_C_DP4	B98	A98	GND
P3E_CPU0_PCIE2_TX_C_DN4	B99	A99	GND
GND	B100	A100	P3E_CPU0_PCIE2_RX_DP3
GND	B101	A101	P3E_CPU0_PCIE2_RX_DN3
P3E_CPU0_PCIE2_TX_C_DP3	B102	A102	GND

P3E_CPU0_PCIE2_TX_C_DN3	B103	A103	GND
GND	B104	A104	P3E_CPU0_PCIE2_RX_DP2
GND	B105	A105	P3E_CPU0_PCIE2_RX_DN2
P3E_CPU0_PCIE2_TX_C_DP2	B106	A106	GND
P3E_CPU0_PCIE2_TX_C_DN2	B107	A107	GND
GND	B108	A108	P3E_CPU0_PCIE2_RX_DP1
GND	B109	A109	P3E_CPU0_PCIE2_RX_DN1
P3E_CPU0_PCIE2_TX_C_DP1	B110	A110	GND
P3E_CPU0_PCIE2_TX_C_DN1	B111	A111	GND
GND	B112	A112	P3E_CPU0_PCIE2_RX_DP0
GND	B113	A113	P3E_CPU0_PCIE2_RX_DN0
P3E_CPU0_PCIE2_TX_C_DP0	B114	A114	GND
P3E_CPU0_PCIE2_TX_C_DN0	B115	A115	GND

3.9.1.2 Riser 2 PINOUT Definition

Table 3-10. PIN definition of PCIe Riser 2

Riser 2			
Name	PIN		Name
P12V	B1	A1	GND
P12V	B2	A2	P12V
P12V	B3	A3	P12V
GND	B4	A4	P12V
P3V3	B5	A5	GND
P3V3	B6	A6	P3V3
P3V3	B7	A7	P3V3
P3V3	B8	A8	P3V3
GND	B9	A9	P3V3
P3V3_AUX	B10	A10	P3V3
IRQ_LVC3_WAKE_N	B11	A11	GND
TP_SLOT2_B12	B12	A12	RST_PERST1_N
SMB_PCI_3V3SB_CLK	B13	A13	SLOT2_PRESENT_N
SM B_PCI_3V3SB_DAT_SLOT2	B14	A14	FM_RISER2_CFG0
GND	B15	A15	FM_RISER2_CFG1
CLK_100M_PE4_DP	B16	A16	GND
CLK_100M_PE4_DN	B17	A17	CLK_100M_PE5_DP

GND	B18	A18	CLK_100M_PE5_DN
CLK_100M_PE6_DP	B19	A19	GND
CLK_100M_PE6_DN	B20	A20	P3E_CPU1_PCIE3_RX_DP8
GND	B21	A21	P3E_CPU1_PCIE3_RX_DN8
P3E_CPU1_PCIE3_TX_C_DP8	B22	A22	GND
P3E_CPU1_PCIE3_TX_C_DN8	B23	A23	GND
GND	B24	A24	P3E_CPU1_PCIE3_RX_DP9
GND	B25	A25	P3E_CPU1_PCIE3_RX_DN9
P3E_CPU1_PCIE3_TX_C_DP9	B26	A26	GND
P3E_CPU1_PCIE3_TX_C_DN9	B27	A27	GND
GND	B28	A28	P3E_CPU1_PCIE3_RX_DP10
GND	B29	A29	P3E_CPU1_PCIE3_RX_DN10
P3E_CPU1_PCIE3_TX_C_DP10	B30	A30	GND
P3E_CPU1_PCIE3_TX_C_DN10	B31	A31	GND
GND	B32	A32	P3E_CPU1_PCIE3_RX_DP11
GND	B33	A33	P3E_CPU1_PCIE3_RX_DN11
P3E_CPU1_PCIE3_TX_C_DP11	B34	A34	GND
P3E_CPU1_PCIE3_TX_C_DN11	B35	A35	GND
GND	B36	A36	P3E_CPU1_PCIE3_RX_DP12
GND	B37	A37	P3E_CPU1_PCIE3_RX_DN12
P3E_CPU1_PCIE3_TX_C_DP12	B38	A38	GND
P3E_CPU1_PCIE3_TX_C_DN12	B39	A39	GND
GND	B40	A40	P3E_CPU1_PCIE3_RX_DP13
GND	B41	A41	P3E_CPU1_PCIE3_RX_DN13
P3E_CPU1_PCIE3_TX_C_DP13	B42	A42	GND
P3E_CPU1_PCIE3_TX_C_DN13	B43	A43	GND
GND	B44	A44	P3E_CPU1_PCIE3_RX_DP14
GND	B45	A45	P3E_CPU1_PCIE3_RX_DN14
P3E_CPU1_PCIE3_TX_C_DP14	B46	A46	GND
P3E_CPU1_PCIE3_TX_C_DN14	B47	A47	GND
GND	B48	A48	P3E_CPU1_PCIE3_RX_DP15
GND	B49	A49	P3E_CPU1_PCIE3_RX_DN15
P3E_CPU1_PCIE3_TX_C_DP15	B50	A50	GND
P3E_CPU1_PCIE3_TX_C_DN15	B51	A51	GND
GND	B52	A52	P3E_CPU1_PCIE2_RX_DP0
GND	B53	A53	P3E_CPU1_PCIE2_RX_DN0

P3E_CPU0_PCIE2_TX_C_DP0	B54	A54	GND
P3E_CPU0_PCIE2_TX_C_DN0	B55	A55	GND
GND	B56	A56	P3E_CPU1_PCIE2_RX_DP1
GND	B57	A57	P3E_CPU1_PCIE2_RX_DN1
P3E_CPU0_PCIE2_TX_C_DP1	B58	A58	GND
P3E_CPU0_PCIE2_TX_C_DN1	B59	A59	GND
GND	B60	A60	P3E_CPU1_PCIE2_RX_DP2
GND	B61	A61	P3E_CPU1_PCIE2_RX_DN2
P3E_CPU0_PCIE2_TX_C_DP2	B62	A62	GND
P3E_CPU0_PCIE2_TX_C_DN2	B63	A63	GND
GND	B64	A64	P3E_CPU1_PCIE2_RX_DP3
GND	B65	A65	P3E_CPU1_PCIE2_RX_DN3
P3E_CPU0_PCIE2_TX_C_DP3	B66	A66	GND
P3E_CPU0_PCIE2_TX_C_DN3	B67	A67	GND
GND	B68	A68	P3E_CPU1_PCIE2_RX_DP4
GND	B69	A69	P3E_CPU1_PCIE2_RX_DN4
P3E_CPU0_PCIE2_TX_C_DP4	B70	A70	GND
P3E_CPU0_PCIE2_TX_C_DN4	B71	A71	GND
GND	B72	A72	P3E_CPU1_PCIE2_RX_DP5
GND	B73	A73	P3E_CPU1_PCIE2_RX_DN5
P3E_CPU0_PCIE2_TX_C_DP5	B74	A74	GND
P3E_CPU0_PCIE2_TX_C_DN5	B75	A75	GND
GND	B76	A76	P3E_CPU1_PCIE2_RX_DP6
GND	B77	A77	P3E_CPU1_PCIE2_RX_DN6
P3E_CPU0_PCIE2_TX_C_DP6	B78	A78	GND
P3E_CPU0_PCIE2_TX_C_DN6	B79	A79	GND
GND	B80	A80	P3E_CPU1_PCIE2_RX_DP7
GND	B81	A81	P3E_CPU1_PCIE2_RX_DN7
P3E_CPU0_PCIE2_TX_C_DP7	B82	A82	GND
P3E_CPU0_PCIE2_TX_C_DN7	B83	A83	GND
GND	B84	A84	P3E_CPU1_PCIE2_RX_DP8
GND	B85	A85	P3E_CPU1_PCIE2_RX_DN8
P3E_CPU0_PCIE2_TX_C_DP8	B86	A86	GND
P3E_CPU0_PCIE2_TX_C_DN8	B87	A87	GND
GND	B88	A88	P3E_CPU1_PCIE2_RX_DP9
GND	B89	A89	P3E_CPU1_PCIE2_RX_DN9

P3E_CPU0_PCIE2_TX_C_DP9	B90	A90	GND
P3E_CPU0_PCIE2_TX_C_DN9	B91	A91	GND
GND	B92	A92	P3E_CPU1_PCIE2_RX_DP10
GND	B93	A93	P3E_CPU1_PCIE2_RX_DN10
P3E_CPU0_PCIE2_TX_C_DP10	B94	A94	GND
P3E_CPU0_PCIE2_TX_C_DN10	B95	A95	GND
GND	B96	A96	P3E_CPU1_PCIE2_RX_DP11
GND	B97	A97	P3E_CPU1_PCIE2_RX_DN11
P3E_CPU0_PCIE2_TX_C_DP11	B98	A98	GND
P3E_CPU0_PCIE2_TX_C_DN11	B99	A99	GND
GND	B100	A100	P3E_CPU1_PCIE2_RX_DP12
GND	B101	A101	P3E_CPU1_PCIE2_RX_DN12
P3E_CPU0_PCIE2_TX_C_DP12	B102	A102	GND
P3E_CPU0_PCIE2_TX_C_DN12	B103	A103	GND
GND	B104	A104	P3E_CPU1_PCIE2_RX_DP13
GND	B105	A105	P3E_CPU1_PCIE2_RX_DN13
P3E_CPU0_PCIE2_TX_C_DP13	B106	A106	GND
P3E_CPU0_PCIE2_TX_C_DN13	B107	A107	GND
GND	B108	A108	P3E_CPU1_PCIE2_RX_DP14
GND	B109	A109	P3E_CPU1_PCIE2_RX_DN14
P3E_CPU0_PCIE2_TX_C_DP14	B110	A110	GND
P3E_CPU0_PCIE2_TX_C_DN14	B111	A111	GND
GND	B112	A112	P3E_CPU1_PCIE2_RX_DP15
GND	B113	A113	P3E_CPU1_PCIE2_RX_DN15
P3E_CPU0_PCIE2_TX_C_DP15	B114	A114	GND
P3E_CPU0_PCIE2_TX_C_DN15	B115	A115	GND

3.9.1.3 OCP MEZZ PINOUT Definition

Table 3-11. PIN definition of PCIe OCP Mezz connector

OCP Mezz			
PIN	Name	PIN	Name
61	P12V	1	MEZZ_PRSNT1_N
62	P12V	2	P5V_AUX
63	P12V	3	P5V_AUX
64	GND	4	P5V_AUX
65	GND	5	GND
66	P3V3_AUX	6	GND
67	GND	7	P3V3_AUX
68	GND	8	GND
69	P3V3	9	GND
70	P3V3	10	P3V3
71	P3V3	11	P3V3
72	P3V3	12	P3V3
73	GND	13	P3V3
74	PU_SMB_LAN_ALERT_N_MEZZ	14	NCSI_OCP_RCSDV
75	SMB_PCI_3V3SB_CLK	15	NCSI_OCP_RCLK
76	SMB_PCI_3V3SB_DAT_MEZZ_R	16	NCSI_OCP_TXEN
77	IRQ_LVC3_WAKE_N	17	RST_PERST0_N
78	NCSI_OCP_RXER	18	TP_OCP_MEZZ_18
79	GND	19	TP_OCP_MEZZ_19
80	NCSI_OCP_TXD0	20	GND
81	NCSI_OCP_TXD1	21	GND
82	GND	22	NCSI_OCP_RXD0
83	GND	23	NCSI_OCP_RXD1
84	CLK_100M_OCP_MEZZA_DP	24	GND
85	CLK_100M_OCP_MEZZA_DN	25	GND
86	GND	26	CLK_100M_OCP_MEZZB_DP
87	GND	27	CLK_100M_OCP_MEZZB_DN
88	P3E_CPU0_PCIE3_TX_C_DP7	28	GND
89	P3E_CPU0_PCIE3_TX_C_DN7	29	GND
90	GND	30	P3E_CPU0_PCIE3_RX_DP7
91	GND	31	P3E_CPU0_PCIE3_RX_DN7
92	P3E_CPU0_PCIE3_TX_C_DP6	32	GND

93	P3E_CPU0_PCIE3_TX_C_DN6	33	GND
94	GND	34	P3E_CPU0_PCIE3_RX_DP6
95	GND	35	P3E_CPU0_PCIE3_RX_DN6
96	P3E_CPU0_PCIE3_TX_C_DP5	36	GND
97	P3E_CPU0_PCIE3_TX_C_DN5	37	GND
98	GND	38	P3E_CPU0_PCIE3_RX_DP5
99	GND	39	P3E_CPU0_PCIE3_RX_DN5
100	P3E_CPU0_PCIE3_TX_C_DP4	40	GND
101	P3E_CPU0_PCIE3_TX_C_DN4	41	GND
102	GND	42	P3E_CPU0_PCIE3_RX_DP4
103	GND	43	P3E_CPU0_PCIE3_RX_DN4
104	P3E_CPU0_PCIE3_TX_C_DP3	44	GND
105	P3E_CPU0_PCIE3_TX_C_DN3	45	GND
106	GND	46	P3E_CPU0_PCIE3_RX_DP3
107	GND	47	P3E_CPU0_PCIE3_RX_DN3
108	P3E_CPU0_PCIE3_TX_C_DP2	48	GND
109	P3E_CPU0_PCIE3_TX_C_DN2	49	GND
110	GND	50	P3E_CPU0_PCIE3_RX_DP2
111	GND	51	P3E_CPU0_PCIE3_RX_DN2
112	P3E_CPU0_PCIE3_TX_C_DP1	52	GND
113	P3E_CPU0_PCIE3_TX_C_DN1	53	GND
114	GND	54	P3E_CPU0_PCIE3_RX_DP1
115	GND	55	P3E_CPU0_PCIE3_RX_DN1
116	P3E_CPU0_PCIE3_TX_C_DP0	56	GND
117	P3E_CPU0_PCIE3_TX_C_DN0	57	GND
118	GND	58	P3E_CPU0_PCIE3_RX_DP0
119	GND	59	P3E_CPU0_PCIE3_RX_DN0
120	OCP_MEZZA_PRSNT_N	60	GND

3.9.1.4 PCIe SSD 0 Pinout Definition

Table 3-12. PIN definition of PCIe SSD0 Connector

PCIe SSD0			
PIN	Name	PIN	Name
A1	SMB_PCI_3V3SB_CLK	C1	CLK_100M_PE7_DP
A2	SMB_PCI_3V3SB_DAT_PESSD0	C2	CLK_100M_PE7_DN
A3	GND	C3	GND
A4	P3E_CPU1_PCIE1_RX_DP1	C4	P3E_CPU1_PCIE1_TX_C_DP1
A5	P3E_CPU1_PCIE1_RX_DN1	C5	P3E_CPU1_PCIE1_TX_C_DN1
A6	GND	C6	GND
A7	P3E_CPU1_PCIE1_RX_DP3	C7	P3E_CPU1_PCIE1_TX_C_DP3
A8	P3E_CPU1_PCIE1_RX_DN3	C8	P3E_CPU1_PCIE1_TX_C_DN3
A9	GND	C9	GND
B1	RST_PERST1_N	D1	SMB_LVC3_PE_HP_SCL_R1
B2	HP_LVC3_PESSD0_PWRGD	D2	SMB_LVC3_PE_HP_SDA_R1
B3	GND	D3	GND
B4	P3E_CPU1_PCIE1_RX_DP0	D4	P3E_CPU1_PCIE1_TX_C_DP0
B5	P3E_CPU1_PCIE1_RX_DN0	D5	P3E_CPU1_PCIE1_TX_C_DN0
B6	GND	D6	GND
B7	P3E_CPU1_PCIE1_RX_DP2	D7	P3E_CPU1_PCIE1_TX_C_DP2
B8	P3E_CPU1_PCIE1_RX_DN2	D8	P3E_CPU1_PCIE1_TX_C_DN2
B9	GND	D9	GND
G1	GND	G3	GND
G2	GND	G4	GND

3.9.1.5 PCIe SSD 1 Pinout Definition

Table 3-13. PIN definition of PCIe SSD1 Connector

PCIe SSD0			
PIN	Name	PIN	Name
A1	SMB_PCI_3V3SB_CLK	C1	CLK_100M_PE8_DP
A2	SMB_PCI_3V3SB_DAT_PESSD1	C2	CLK_100M_PE8_DN
A3	GND	C3	GND
A4	P3E_CPU1_PCIE1_RX_DP5	C4	P3E_CPU1_PCIE1_TX_C_DP5
A5	P3E_CPU1_PCIE1_RX_DN5	C5	P3E_CPU1_PCIE1_TX_C_DN5
A6	GND	C6	GND
A7	P3E_CPU1_PCIE1_RX_DP7	C7	P3E_CPU1_PCIE1_TX_C_DP7
A8	P3E_CPU1_PCIE1_RX_DN7	C8	P3E_CPU1_PCIE1_TX_C_DN7
A9	GND	C9	GND
B1	RST_PERST1_N	D1	SMB_LVC3_PE_HP_SCL_R2
B2	HP_LVC3_PESSD1_PWRGD	D2	SMB_LVC3_PE_HP_SDA_R2
B3	GND	D3	GND
B4	P3E_CPU1_PCIE1_RX_DP4	D4	P3E_CPU1_PCIE1_TX_C_DP4
B5	P3E_CPU1_PCIE1_RX_DN4	D5	P3E_CPU1_PCIE1_TX_C_DN4
B6	GND	D6	GND
B7	P3E_CPU1_PCIE1_RX_DP6	D7	P3E_CPU1_PCIE1 TX_C_DP6
B8	P3E_CPU1_PCIE1_RX_DN6	D8	P3E_CPU1_PCIE1 TX_C_DN6
B9	GND	D9	GND
G1	GND	G3	GND
G2	GND	G4	GND

3.10 LAN ON MOTHERBOARD (LOM)

The baseboards will use the Intel® I350 code named Powerville Dual 10/100/1000 integrated MAC and PHY controller. The Powerville LAN controller requires a PCIe x4 Gen2 upstream interface. The Powerville controller also requires the use of the Wellsburg SMBus interface during Sleep states S5 as well as for ME Firmware. The Powerville LAN controller will be on standby power so that Wake on LAN and manageability functions can be supported. Powerville will be used in conjunction with the BMC for out of band Management traffic. The BMC will communicate with Powerville over a NC-SI interface (RMII physical). Powerville will be on standby power so that the BMC can send management traffic over the NC-SI interface to the network during sleep states S5.

3.10.1 DEDICATED NIC (MANAGEMENT RJ45 Port)

Motherboards will support embedded version of the Dedicated NIC. The Dedicated NIC feature provides a dedicated 1G/100M/10Mb Ethernet interface for remote management features. The Dedicated NIC consists of a 1G/100M/10MbE PHY device which interfaces to the primary NC-SI port 0 (RGMII mode) out of the AST2400 integrated BMC, to offer a dedicated management 1G/100M/10MbE port. Because of the limited distance the RGMII signals can travel, the recommended placement for this connector is to be as close as possible to the AST2400 IBMC.

3.11 LPC BUS

The PCH implements an LPC interface as described in the Low Pin Count Interface Specification, Revision 1.1. The PCH LPC bus is used to connect to the BMC and to an optional TPM device.

3.12 TPM

The PCH supports TPM specification 1.2 level2 revisions 103. The Baseboard will not be populated with a TPM device except for special deals that require a TPM.

3.13 SERIAL PORT

There are two serial ports provided. One is external serial port on rear. One is internal serial port. The usage is either debug or for a terminal concentrator. Since the serial port does not exist in the IO panel, the user will need to use a cable and chassis knock out for a DB9 connector. The cable will connect to a standard 10 pin serial port header. Note that the choice of RS232 transceivers is limited by the absence of a -12V rail.

3.14 FANs

The board supports a total **8** FANs. Fan signals are made available via a consolidated header. The FAN control and FAN speed monitor are from BMC chip. BMC will have FAN Tachometer and PWM function. Note that all fans will operate at the same speed.

3.15 Jumper Definition

Below table is Jumper definition of board.

Table 4-7 BIOS/BMC Jumper Setting

JUMPER LOCATION		DEFAULT SETTING.	FUNCTION
PASSWORLD CLEAR	JP11	1-2	1-2 : HOLD (DEFAULT) 2-3 : CLEAR
RECOVER BIOS JUMPER	JP1	1-2	1-2 : HOLD (DEFAULT) 2-3 : RECOVER BIOS
CLR RTC_RST	JP10	1-2	1-2 : HOLD (DEFAULT) 2-3 : CLR RTC_RST
ME FIRMWARE UPDATE	JP8	1-2	1-2 : HOLD (DEFAULT) 2-3 : ME IN FORCE UPDATE MODE
BMC Disable/Enable	J19	1-2	Open: HOLD (DEFAULT) 1-2: Disable BMC
SOL Enable	J7	1-2	Open: HOLD (DEFAULT) 1-2: Enable BMC
Intruder Enable	J57	1-2	Open: HOLD (DEFAULT) 1-2: Chassis Top Covered
SMB_SML0 debug header	JP24	Pin1 Pin3	Pin1: Smb_Sml0_3V3sb_Clk Pin3: Smb_Sml0_3V3sb_Dat
SMB Host debug header	JP7	Pin1 Pin3	Pin1: Smb_Host_3V3sb_Clk Pin3: Smb_Host_3V3sb_Dat
SMB_PMbus Debug Header	JP2	Pin1 Pin3	Pin1: Smb_3V3sb_Pmbus_Clk Pin3: Smb_3V3sb_Pmbus_Dat

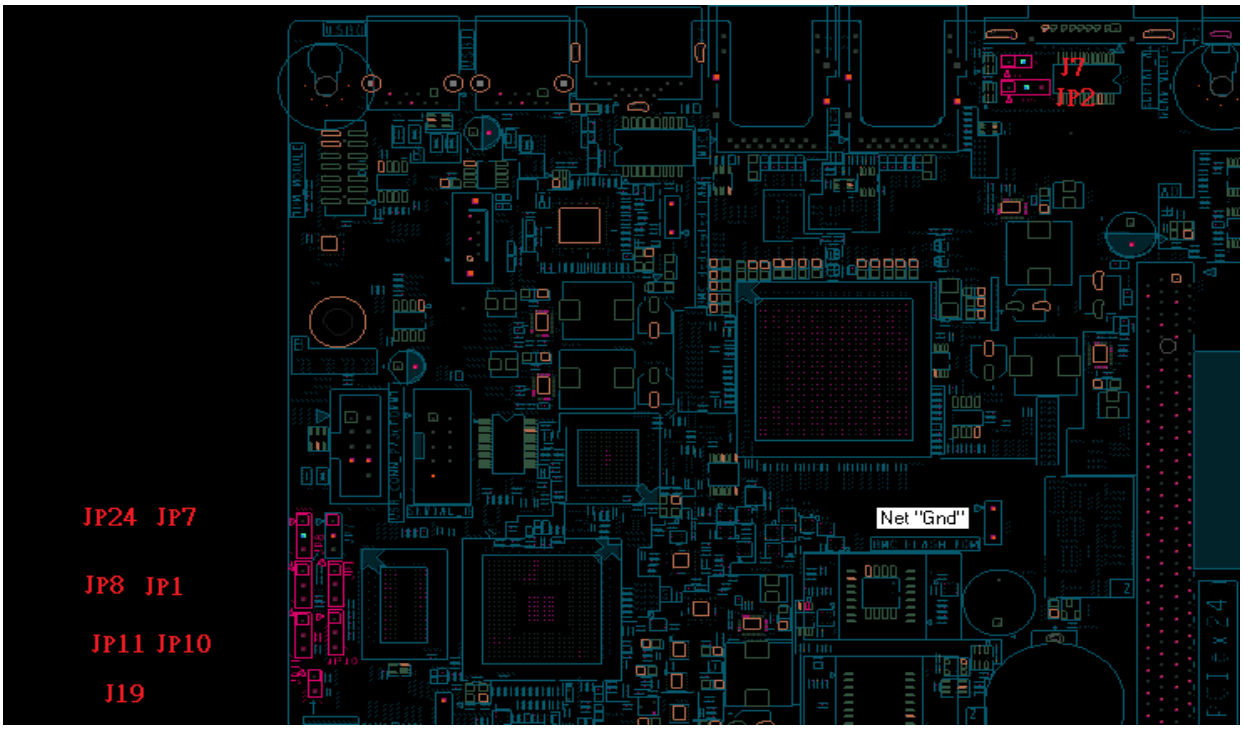

Figure 3-18: Jumper Location

3.15.1 Password Clear

The user sets this 3-pin jumper to clear the password. The pin should be strapped LOW when the password needs to be reset.

Table 4-8 Password Clear Jumper

Jumper Position	Mode of Operation	Note
1-2	Normal	FM_PASSWORD_CLEAR_N pin is pulled HIGH. Default position.
2-3	Clear Password	FM_PASSWORD_CLEAR_N pin is pulled LOW.

3.16 DEBUG header Information

3.16.1 XDP SUPPORT

Standard XDP header for Grantley-EP Processors (XDP 0) will be provided, the XDP connector will be depopulated in production, please indicate parts that can be safely removed for production in the schematic.

3.16.2 SMB Debug Header (JP7)

SMB Debug Header is a SMB debug header which was connected to PCH's HOST channel and BMC SMB channel 4.

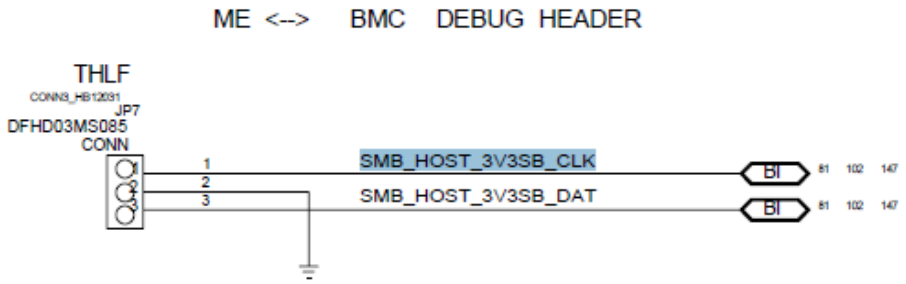

Figure 3-19: S2B SMB debug Header

3.16.3 BMC Debug Header (JP2 and J19)

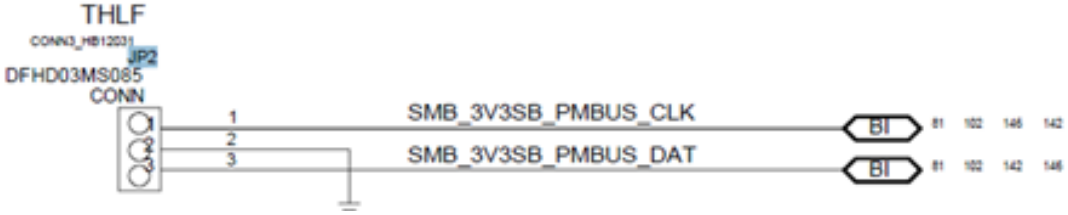

Figure 3-20: S2B PMBUS debug Header

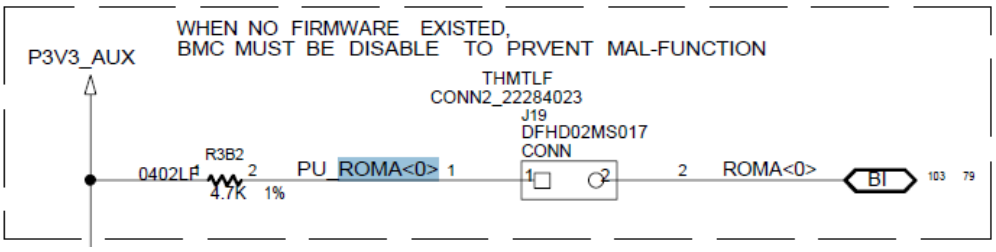

Figure 3-21: S2B BMC Desiable Header

3.17 PRODUCT SENSORS

Table 3-15. Baseboard Sensor list

	Description	
TMP75_0	Temperature sensor on middle of board	PCI_Inlet_Temp2
TMP75_1	Temperature sensor close to OCP Mezz	PCI_Inlet_Temp1
TMP75_2	Temperature sensor close to dedicated NIC	Exhaust_Temp
AST2400 (BMC)	Monitor CPU core voltage and system voltage	

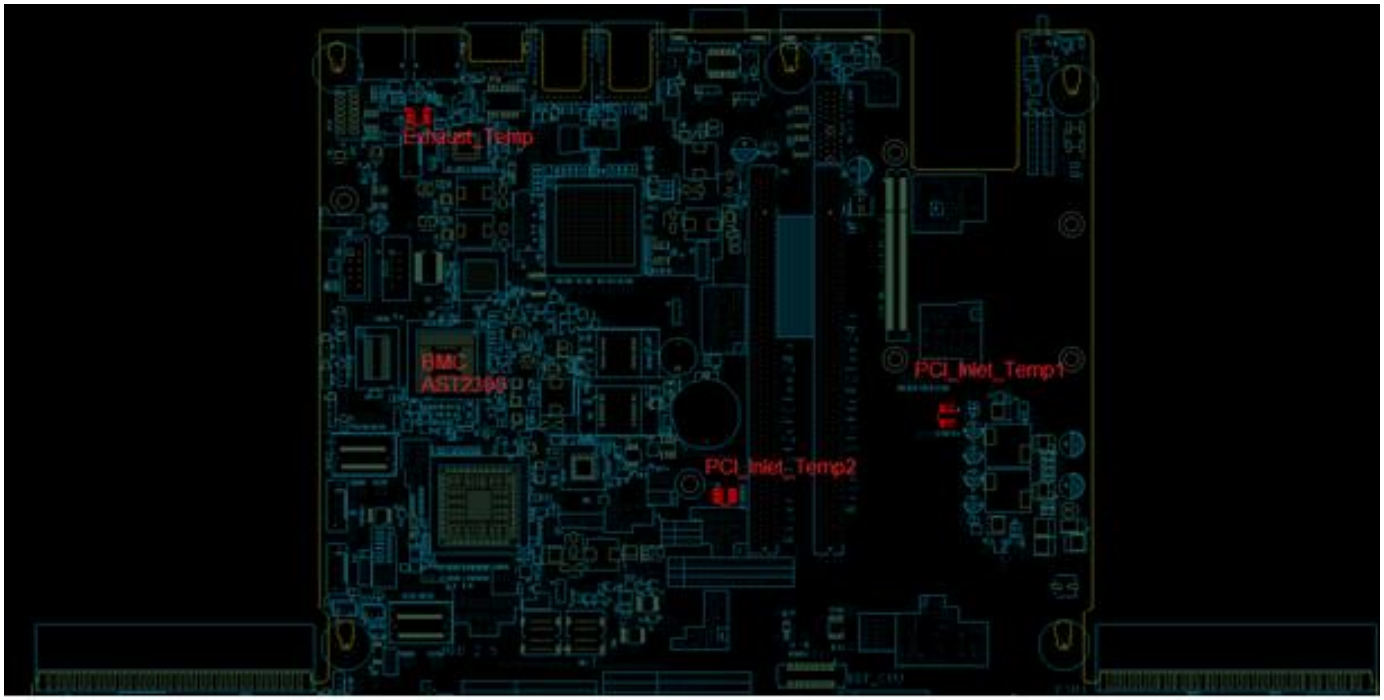

Figure 3-22: S2B Temperature sensor

3.18 SMBUS

The products must comply with the Grantley Platform common-core SMBUS architecture in order to maximize BIOS, Wellsburg ME Firmware, and BMC firmware. This is a requirement in an order to minimize BIOS and Firmware code development efforts and improve validation and product board stability and debugging.

Figure 3-23: Grantley BMC SMBUS Block Diagram

3.19 POWER

These are max values (where available) for board VR design purposes. From a system power supply budgeting or thermal standpoint it's recommended to apply a derating factor. TDP power estimate for the main components are provided in below table as well.

3.19.1.1 LED Behavior of POWER SUPPLY

LED TABLE

Condition: Standby Mode / Single unit	
Status	**LED**
normal	**Green**
Fan lock (15 sec)	**Yellow**

Power Unit	Condition	Status	LED
Single unit	Standby Mode	normal	Green
		Fan Lock(15 sec)	Yellow
		OTP	Green
	Normal Mode	normal	Green
		Fan Lock(15 sec)	Yellow
		OTP	Yellow
		OCP	Yellow
		OVP	Yellow
		UVP	Yellow
Two units	Standby Mode (one unit NO AC)	normal	No light
		Fan Lock(15 sec)	No light
		OTP	No light
	Standby Mode	normal	Green
		Fan Lock(15 sec)	Yellow
		OTP	Green
	Normal Mode	normal	Green
		Fan Lock(15 sec)	Yellow
		OTP	Yellow
		OCP	Yellow
		OVP	Yellow
		UVP	Yellow

Table 3-17. LED Behavior of PSU

3.19.2 Power supply PINOUT

Table 3-17. PIN definition of Power Supply 0

Power Supply 0			
Name	PIN		Name
P12V	64	1	P12V
P12V	63	2	P12V
P12V	62	3	P12V
P12V	61	4	P12V
P12V	60	5	P12V
P12V	59	6	P12V
P12V	58	7	P12V
P12V	57	8	P12V
P12V	56	9	P12V
P12V	55	10	P12V
P12V	54	11	P12V
P12V	53	12	P12V
GND	52	13	GND
GND	51	14	GND
GND	50	15	GND
GND	49	16	GND
GND	48	17	GND
GND	47	18	GND
GND	46	19	GND
GND	45	20	GND
GND	44	21	GND
GND	43	22	GND
GND	42	23	GND
GND	41	24	GND
PSU_REMOTE_SENSE_P	40	25	TP_TACH
P12V_STBY	39	26	PSU_REMOTE_SENSE_N
PSU_A0	38	27	TP_VIN_GOOD
PWROK0	37	28	CSHARE
GND	36	29	FM_PS_EN_PSU_N
SMB_3V3SB_PMBUS_CLK	35	30	PS_KILL_0

PSU_PRESENT0_N	34	31	RESET_PS_0
SMB_3V3SB_PMBUS_DAT	33	32	IRQ_SML1_PMBUS_ALERT_N

Table 3-18. PIN definition of Power Supply 1

Power Supply 1			
Name	PIN		Name
P12V	64	1	P12V
P12V	63	2	P12V
P12V	62	3	P12V
P12V	61	4	P12V
P12V	60	5	P12V
P12V	59	6	P12V
P12V	58	7	P12V
P12V	57	8	P12V
P12V	56	9	P12V
P12V	55	10	P12V
P12V	54	11	P12V
P12V	53	12	P12V
GND	52	13	GND
GND	51	14	GND
GND	50	15	GND
GND	49	16	GND
GND	48	17	GND
GND	47	18	GND
GND	46	19	GND
GND	45	20	GND
GND	44	21	GND
GND	43	22	GND
GND	42	23	GND
GND	41	24	GND
PSU_REMOTE_SENSE_P	40	25	TP_TACH
P12V_STBY	39	26	PSU_REMOTE_SENSE_N
PSU_A1	38	27	TP_VIN_GOOD
PWROK1	37	28	CSHARE
GND	36	29	FM_PS_EN_PSU_N

SMB_3V3SB_PMBUS_CLK	35	30	PS_KILL_1
PSU_PRESENT1_N	34	31	RESET_PS_1
SMB_3V3SB_PMBUS_DAT	33	32	IRQ_SML1_PMBUS_ALERT_N

4 PRODUCT SYSTEM REQUIREMENTS

1U and 2U chassis will be enabled to complement the board offering. A new chassis development is expected in order to accommodate the marketing requirements of a spread-core form factor and the docking power supplies.

4.1 Chassis Overview

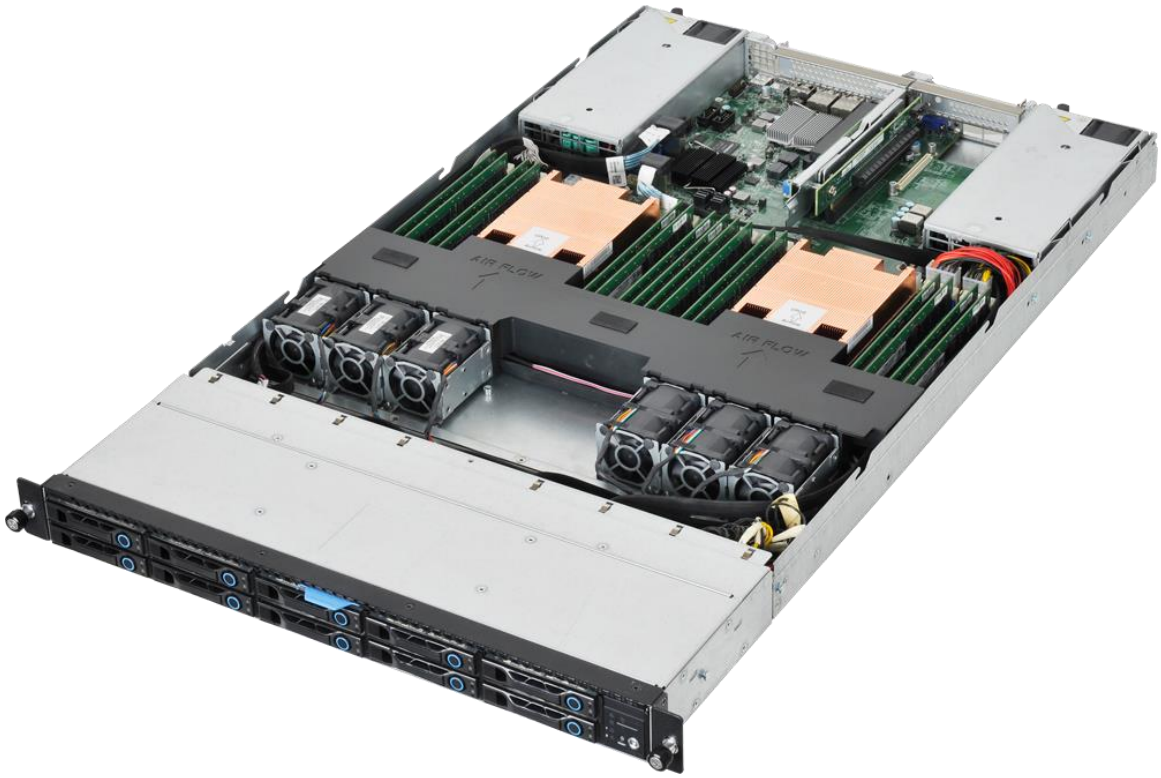

Figure 4-1 1U Chassis

Figure 4-2 1U Chassis Front and Rear View

4.2 LED behavior

4.2.1 Front Panel LED Function and Behavior

4.2.1.1 2U System

Table 4-1. LED behavior of 2U system

Mark	Name	Color	Condition	Behavior	Voltage	Owner
	Power LED	Blue	On	S0 System Power On	5VSB	BMC
			OFF	S5 System Power Off		
	ID LED	Blue	Blinking	Unit selected for Identification	5VSB	BMC
			OFF	No Identificaiton requested		
	Fault LED	Amber	Blinking	Critical Failure: FAN /Temp/ Voltage	5VSB	BMC
				Non Critical Failure:		
			OFF	SEL Cleared		
				Last pending warning or Error has been deleted		
	HDD Activity	Blue	Blinking	HDD access (SATA Onboard Only)	5V	PCH
			OFF			
	LAN1 LED	Blue	ON	Link	3V3AUX	LAN1
		Blue	Blinking	LAN Access		
	LAN2 LED	Blue	ON	Link	3V3AUX	Lan2
		Blue	Blinking	LAN Access		